

Fig. 1

<u>Inst</u>	<u>Hit/Miss</u>	<u>Data</u>	
18 — LDR [R <sub>m</sub> ]	Hit	Data [R <sub>m</sub> ]	
MOV	N/A	—	
CMP	N/A	—	
⋮	⋮	⋮	
20 — LDR [R <sub>m</sub> ]	Miss	—	<div> <div></div> <div>variable delay</div> <div></div> </div>
MOV	N/A	—	
CMP	N/A	Data [R <sub>m</sub> ]	
⋮			
22 — LDR [R1]	Miss	—	
24 — LDR [R2]	Miss	—	
MOV	N/A	—	
CMP	N/A	28 — Data [R2]	<div> <div></div> <div>missed data returned out of order</div> <div></div> </div>
ADD	N/A	26 — Data [R1]	

Fig. 2

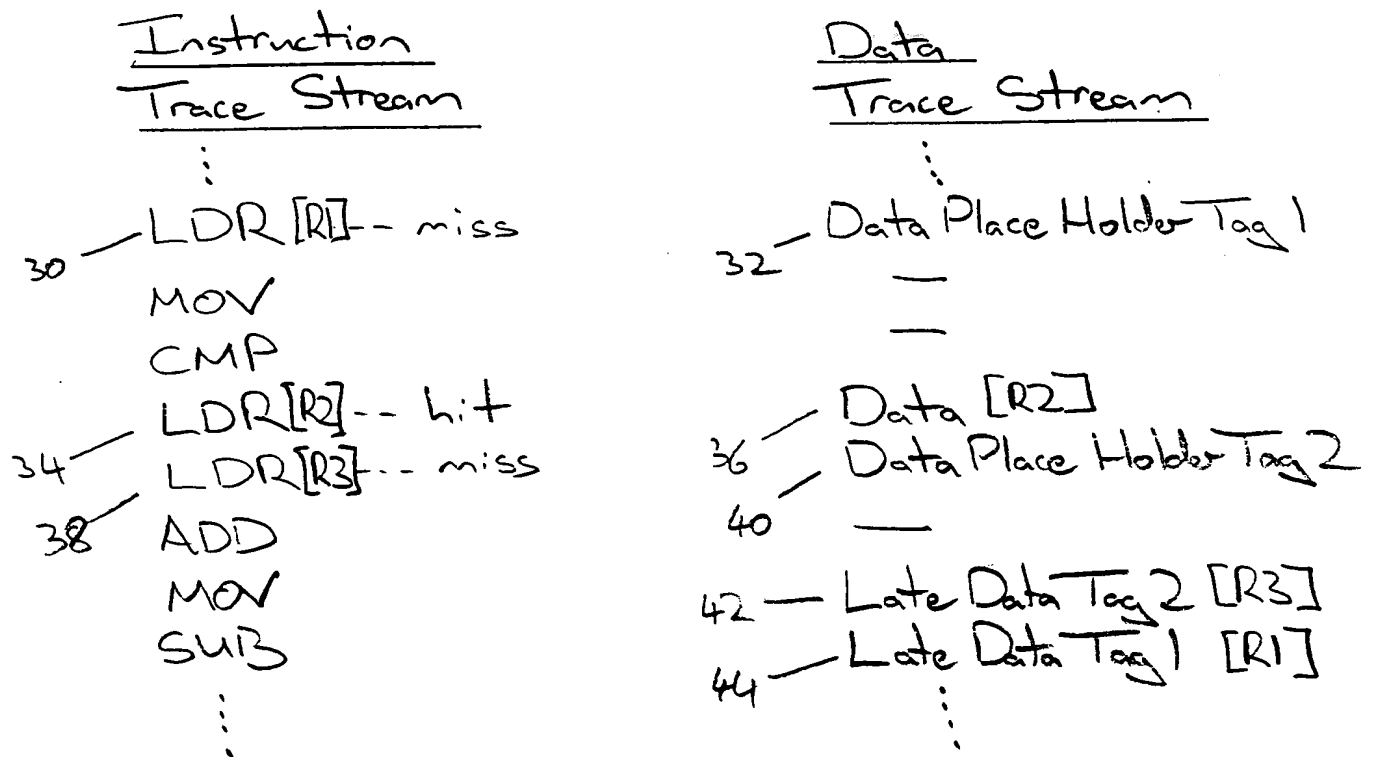


Fig. 3

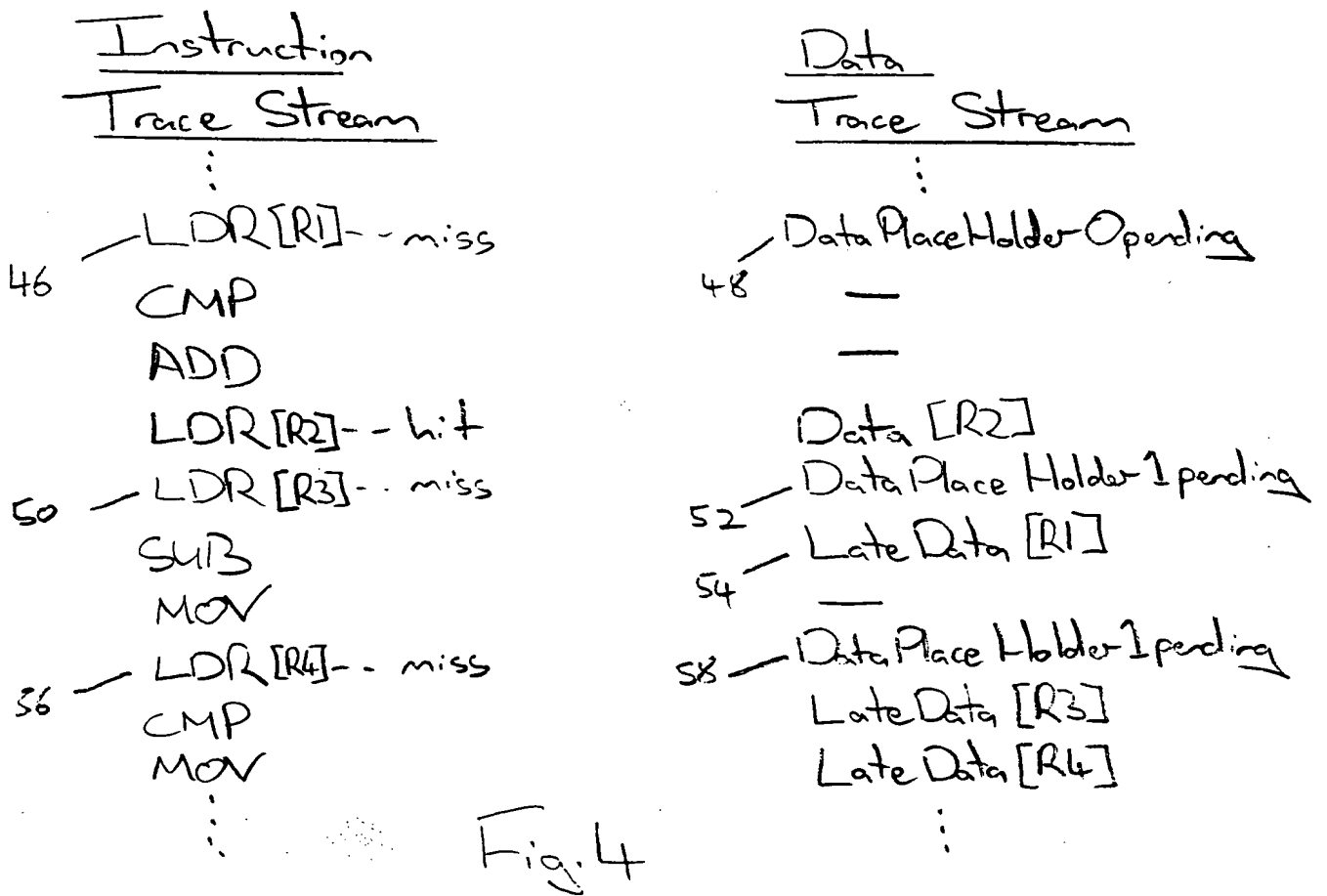


Fig. 4

# Instruction Trace Stream

62 (LDR [R1] --- miss)  
 (MOV)  
 SUB  
 ↓  
 earliest trace info.  
 SYNC {1 pending}  
 60 LDR [R2] --- miss  
 CMP  
 ADD  
 64 LDR [R3] --- hit  
 MOV  
 SUB  
 CMP  
 ...  
 ...

# Data Trace Stream

(Data Placeholder)

—  
 —  
 —  
 66 Data Placeholder  
~~Late Data [R1]~~  
 68 —  
 —  
 Data [R3]  
 Late Data [R2]  
 70 —  
 —  
 ...  
 ...

Fig. 5

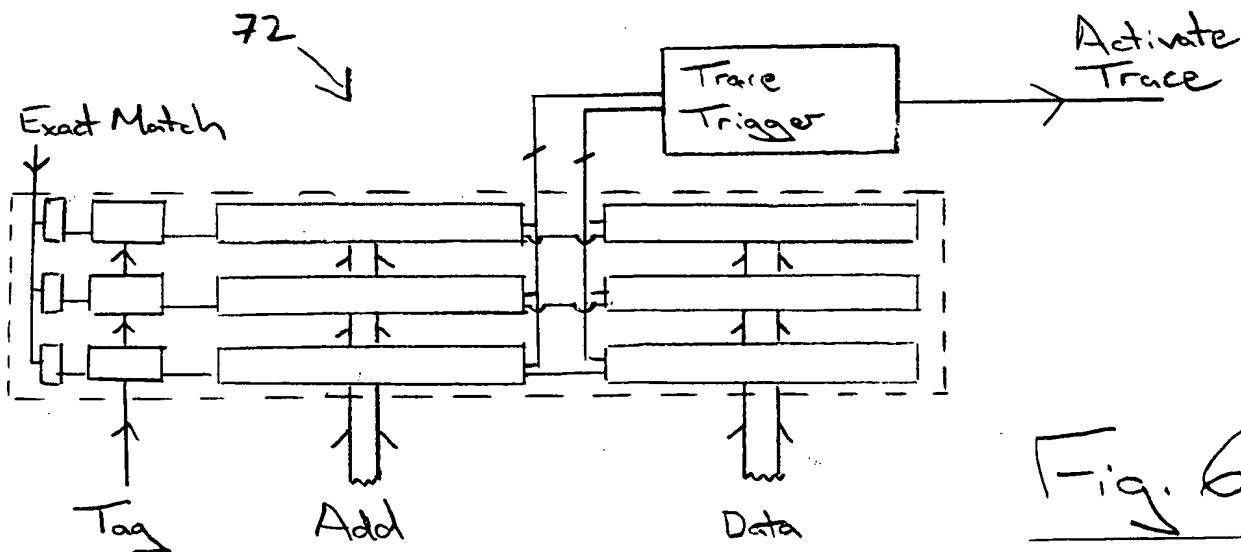


Fig. 6

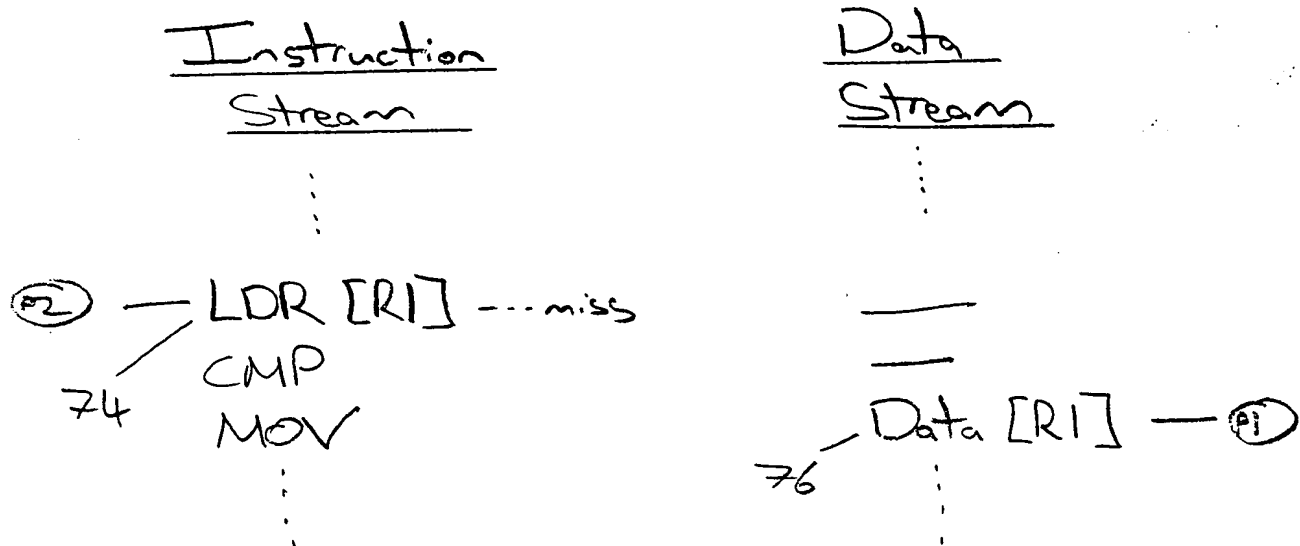


Fig. 7

Exact Match	Add Match	Data Match	Trace Activation Point
✓	✓	✓	①
✓	✓	X	none
X	✓	✓	②
X	✓	X	②

Fig. 8

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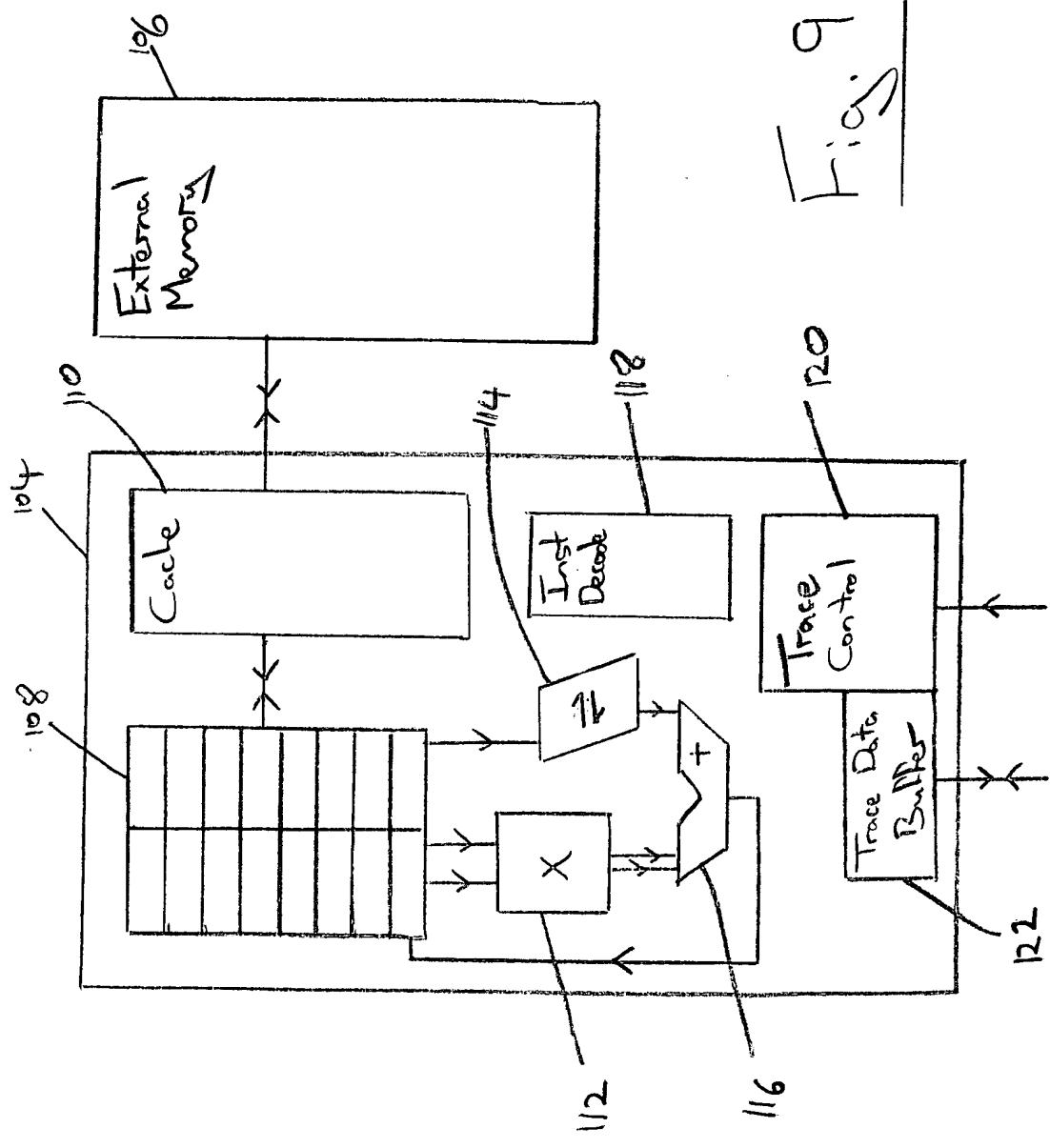


Fig. 9

LSM  $R_n[Add]$ ,  $RegList$

16 bits

0000100010001011



R0	
R1	
R3	R11
R7	

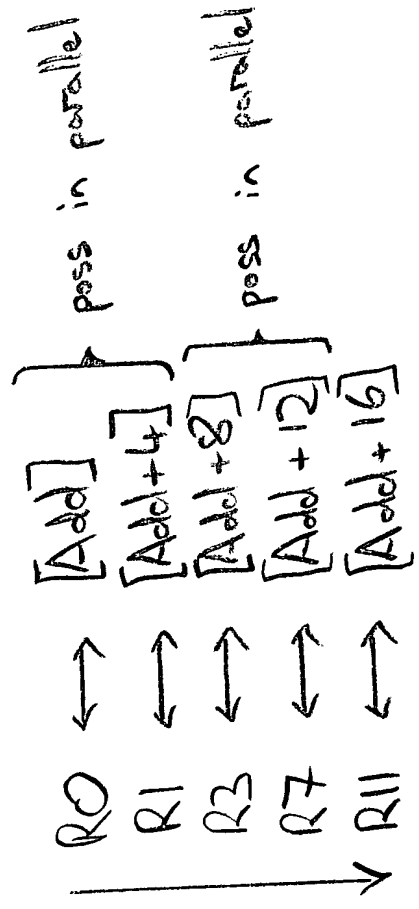


Fig. 10

$$R0 \xleftrightarrow{DW_1} [Add]$$

$$R1 \xleftrightarrow{DW_2} [Add+4]$$

$$R3 \xleftrightarrow{DW_3^*} [Add+8]!$$

$$R7 \xleftrightarrow{DW_4} [Add+12]$$

$$R11 \xleftrightarrow{DW_5} [Add+16]$$

Trace  
Triggers

Trace  
to  
End

$\gg$

Trace Data Stream

..., {LSM}, {Add+8}, {DW3}, {Place Holder}, {Place Holder}, ...

Count back to R3

Fig. 11



Fig. 12

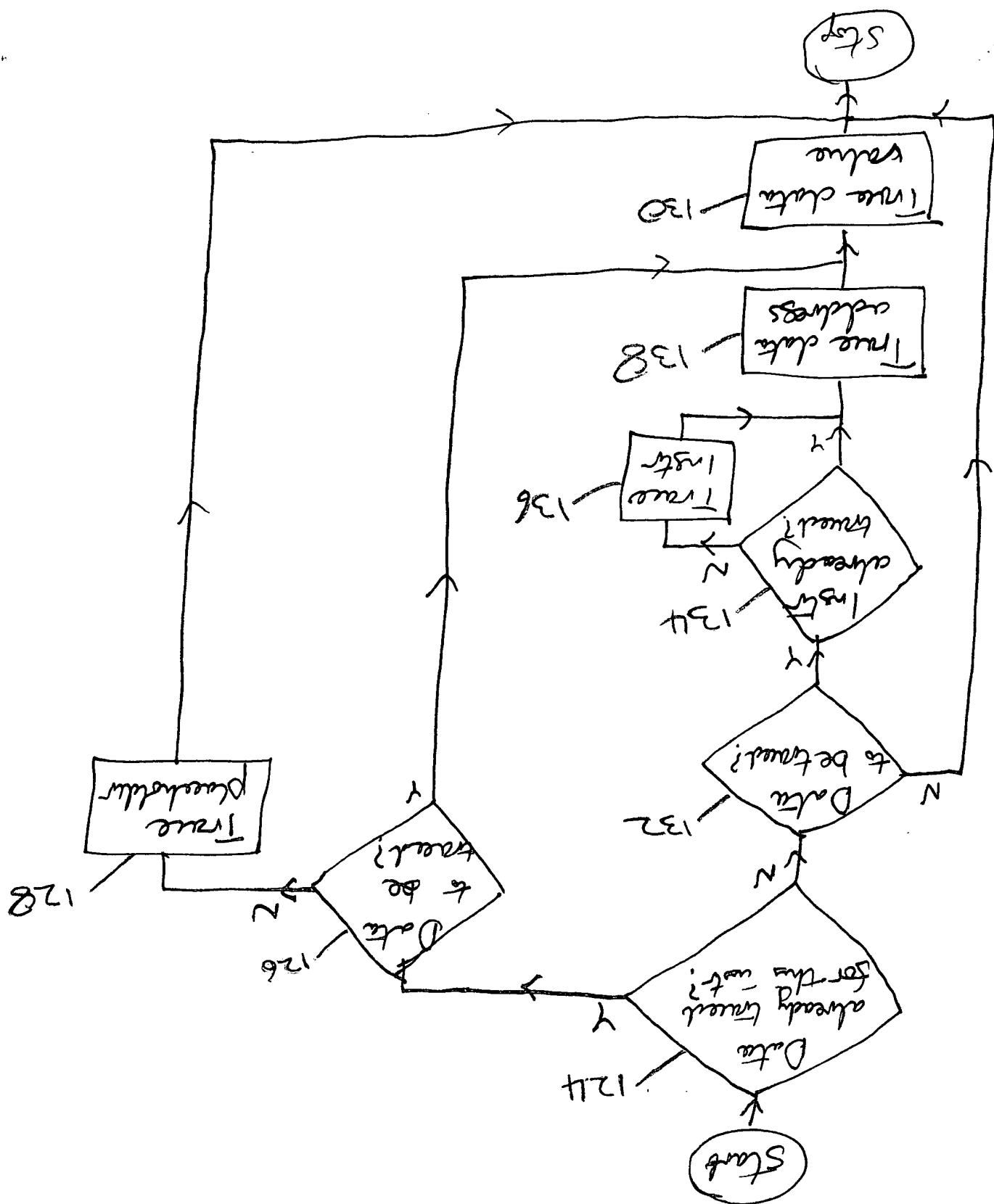


Fig. 13

